

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

David Hoyle

Serial No: 09/703,140

Filed: October 31, 2000

For: Microprocessor With Rounding Multiply Instructions

Docket No.: TI-30554

Art Unit: 2124

Examiner: Mai, Tan V.

Conf. No.: 1023

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LETTER TO THE OFFICIAL DRAFTPERSON

Technology Center 2100

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Dear Sir:

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(a)

I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on March 10, 2004

Indranil Chowdhury
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Please find enclosed the formal drawings for the subject case. Charge any necessary fees to Deposit Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,

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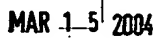
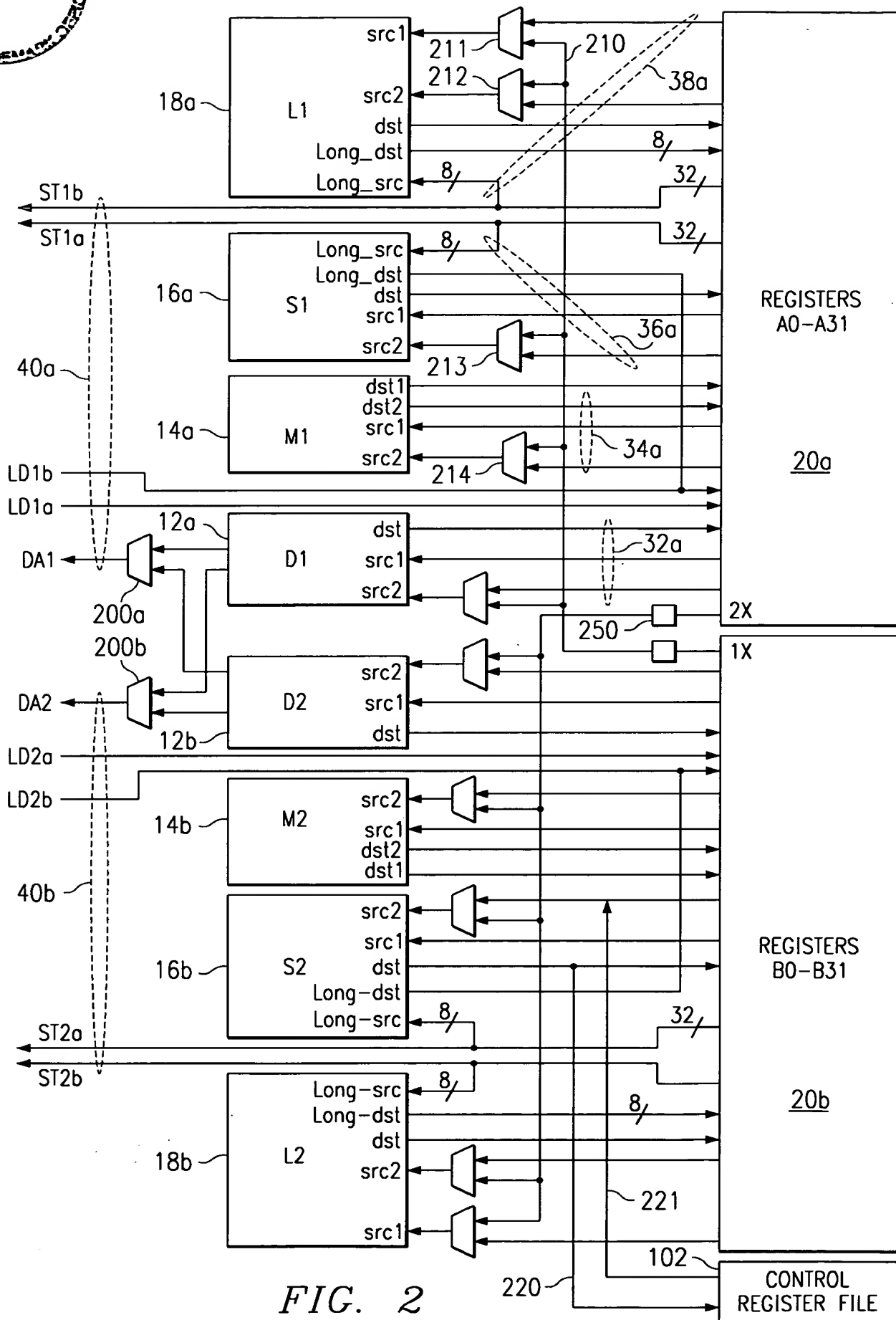
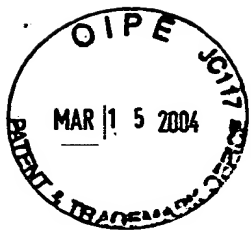


FIG. 1





OPERATIONS ON THE .L UNIT

31	29	28	27	23	22	18	17	13	12	11	5	4	3	2	1	0
CREG	Z	DST	SCR2	SRC1/CST	X	OP										
3	5	5	5	5	5	7										

FIG. 3A

OPERATIONS ON THE .M UNIT

31	29	28	27	23	22	18	17	13	12	11	7	6	5	4	3	2	1	0
CREG	Z	DST	SCR2	SRC1/CST	X	OP												
3	5	5	5	5	5	5												

FIG. 3B

OPERATIONS ON THE .D UNIT

31	29	28	27	23	22	18	17	13	12	7	6	5	4	3	2	1	0
CREG	Z	DST	SCR2	SRC1/CST	OP												
3	5	5	5	5	5	6											

FIG. 3C

LOAD/STORE WITH 15-BIT OFFSET (ON THE .D UNIT)

31	29	28	27	23	22	8	7	6	4	3	2	1	0
CREG	Z	DST/SRC	UCST15	Y	LD/ST	1	1	S	P				
3	5	5	15	3									

FIG. 3D

LOAD/STORE 'BASER' + 'OFFSETR/CST' ON THE .D UNIT

31	29	28	27	23	22	18,17	13	12	9	8	7	6	4	3	2	1	0
CREG	Z	DST/SRC	BASE R	OFFSET R/UCST5	MODE	R	Y	LD/ST	0	1	S	P					
3	5	5	5	5	4												

FIG. 3E



OPERATIONS ON THE .S UNIT

31	29	28	27	23	22	18	17	13	12	11	6	5	4	3	2	1	0
CREG	Z		DST			SRC2		SRC1/CST	X		OP		0	0	0	0	S P
3			5			5			5			6					

FIG. 3F

ADDK ON THE .S UNIT

31	29	28	27	23	22	7	6	5	4	3	2	1	0
CREG	Z		DST						1	0	1	0	S P
3			5			16							

FIG. 3G

BITFIELD OPERATIONS (IMMEDIATE FORMS) ON THE .S UNIT

31	29	28	27	23	22	18	17	13	12	8	7	6	5	4	3	2	1	0								
CREG · Z		DST				SRC2		CSTA		CSTB		OP		0		0		1		0		S		P		
3			5			5			5			2														

FIG. 3H

MVK AND MVKH ON THE .S UNIT

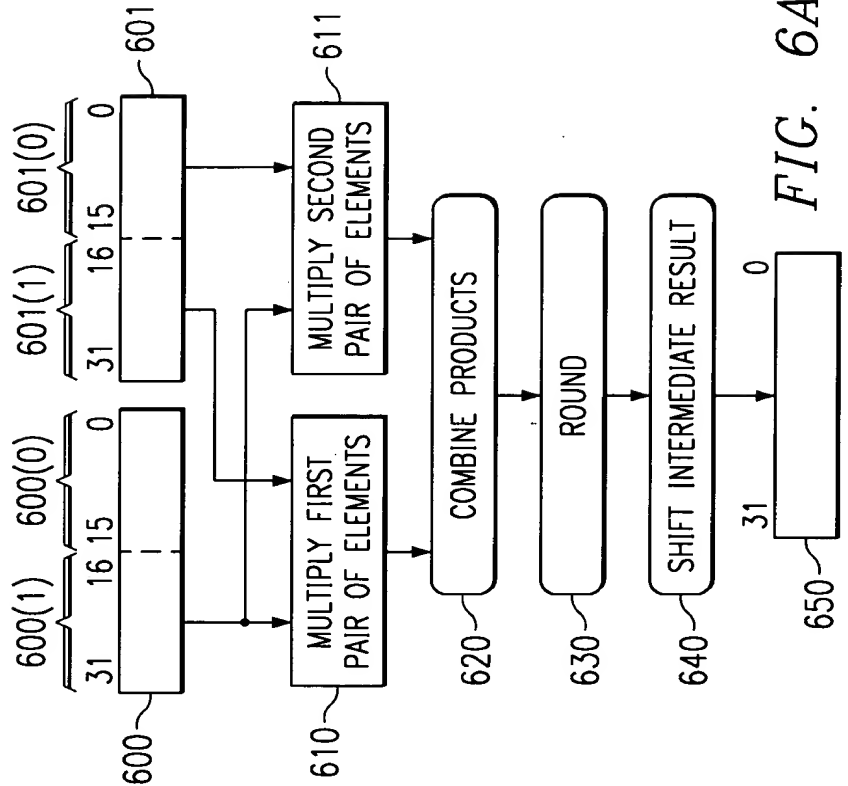
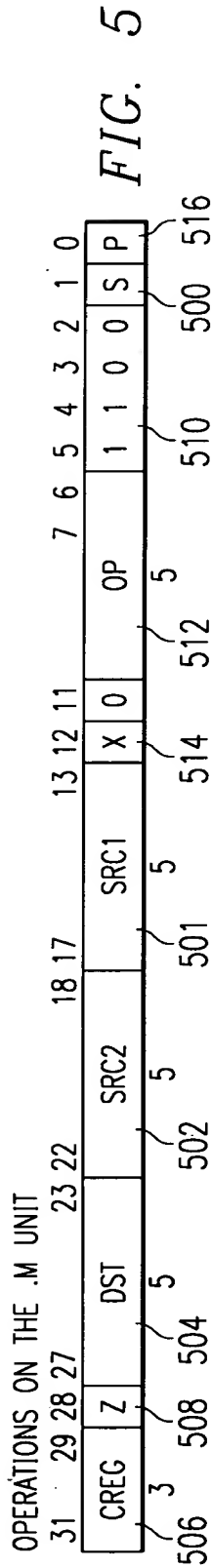
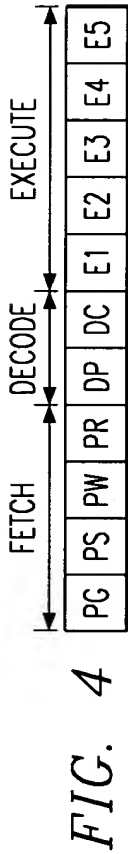
31	29	28	27	23	22	7	6	5	4	3	2	1	0
CREG	Z		DST						H	1	0	1	S P
3			5			16							

FIG. 3I

BCOND DISP ON THE .S UNIT

31	29	28	27	7	6	5	4	3	2	1	0
CREG	Z							0	0	1	S P
3			21								

FIG. 3J



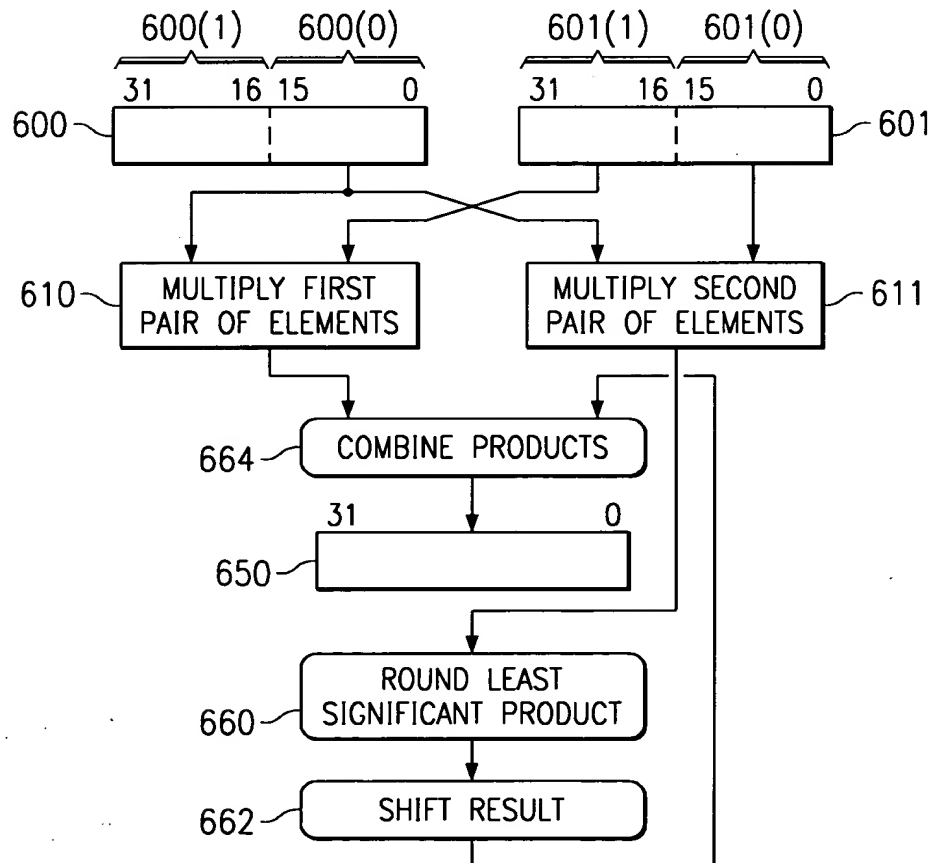
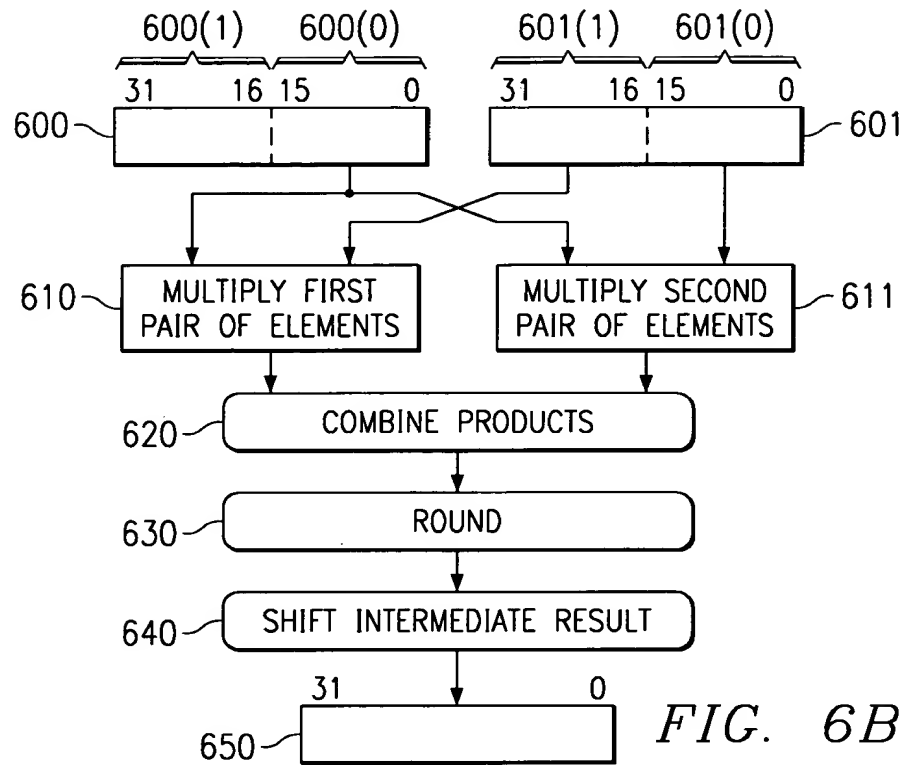


FIG. 6C

FIG. 7A

Block diagram of a 64-bit floating-point multiplier. The diagram shows a multi-stage pipeline with three main paths: a left path for saturation and zero detection, a middle path for general multiplication, and a right path for MPY (multiply) operations.

Left Path (Saturation and Zero Detection):

- SATURATE LOGIC (735):** Receives SAT input.
- DST1_MUX w/ ZERO_DETECT (734):** Receives DST1 and ZERO1 inputs.
- DST2_MUX w/ ZERO_DETECT (734):** Receives DST2 and ZERO2 inputs.

Middle Path (General Multiplication):

- NON-MPY SRC1/SRC2 LATCHES (730a):** Receives SRC1 and SRC2 inputs.
- 730:** A block containing SWIZZLE NETWORK, AVG, BITC, and ROT/SSHVL/SSHVR.
- NON-MPY E1 LOGIC (700a):** Receives output from 730.
- PIPELINE REGISTERS (731a):** Receives output from 700a.
- ROT/SSHVL/SSHVR E2 LOGIC (731a):** Receives output from 731a.
- GMPY/MVD E2 LOGIC (700b):** Receives output from 731a.
- PIPELINE REGISTERS (732a):** Receives output from 700b.
- GMPY/MVD E3 LOGIC (700c):** Receives output from 732a.
- PIPELINE REGISTERS (733a):** Receives output from 700c.
- (63:0) and (63:32) outputs:** The final 64-bit result is split into two 32-bit outputs.

Right Path (MPY Operations):

- MPY SRC1/SRC2 LATCHES (711):** Receives SRC1 and SRC2 inputs.
- MULT ARRAY(2) (711b, 711a):** Receives output from 711.
- PIPELINE REGISTERS (731b):** Receives output from 711b.
- MPY/AVG E2 LOGIC (732b):** Contains AVG2/AVGU4/MPY 8/16/32 BIT ADDER and 16/32 BIT ADDER.
- PIPELINE REGISTERS (733b):** Receives output from 732b.
- MPY E3 LOGIC (733c):** Contains 16/32/48 BIT ADDER.
- PIPELINE REGISTERS (733c):** Receives output from 733c.
- INCREMENTER (710):** Receives output from 733c.
- 17 BIT ADDER (710):** Receives output from 710.

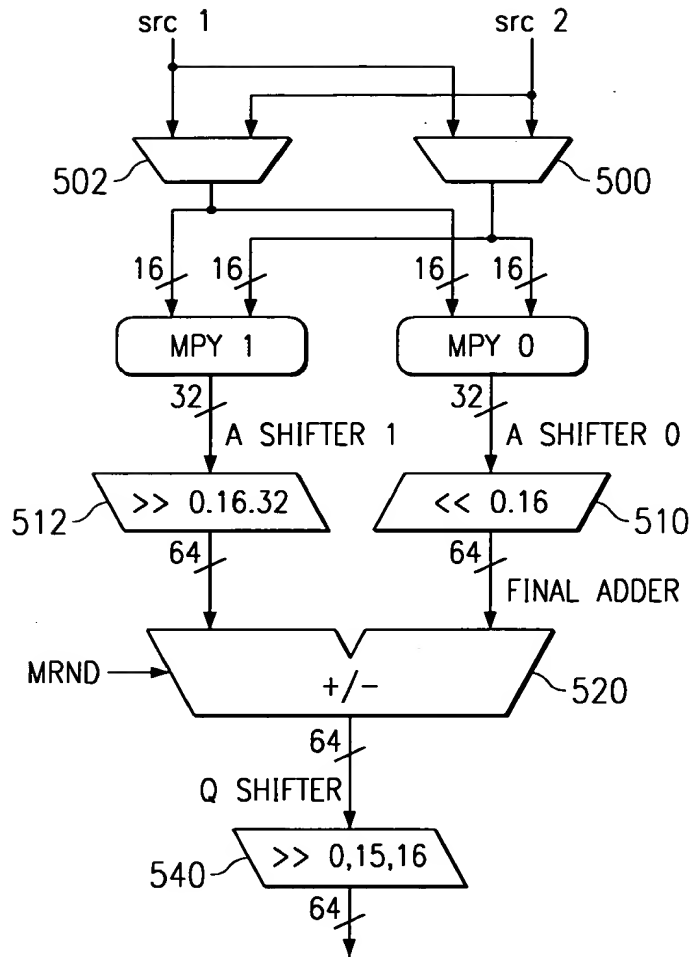
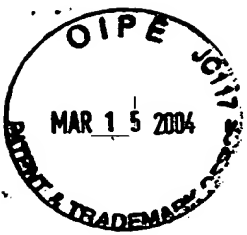


FIG. 7B

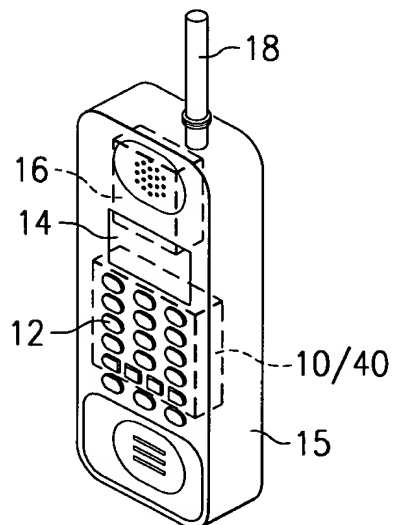


FIG. 8